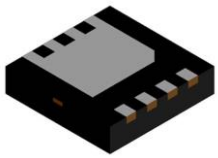
# SNM1021DRA

## Single N-Channel, 100V, 31A, Power MOSFET

http://www.sitcores.com/

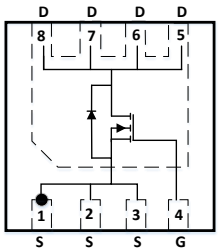
| $V_{DS}$ (V) | Max.$R_{DS(on)}$ (mΩ) |
|---|---|
| 100 | 21@ $V_{GS}$= 10V |
| | 34@ $V_{GS}$= 4.5V |



DFN3333-8L

## Description

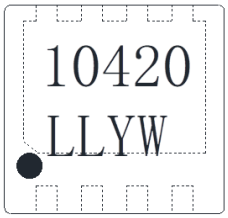
The SNM1021DRA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced Split Gate Trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM1021DRA is in compliance with RoHS.




Pin configuration (Top view)

## Features

- Split Gate Trench technology
- Supper high density cell design
- Low ON resistance
- 100% UIS and Rg Tested
- MSL3




10420 = Device Code
LL = Special Code
Y = Year
W = Week (A~z)

Marking

## Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

## Order information

| Device | Package | Shipping |
|---|---|---|
| SNM1021DRA-8/TR | DFN3333-8L | 3000/Tape&Reel |

## Absolute Maximum ratings

| Parameter | | Symbol | Maximum | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain Current | $T_C$=25°C | $I_D$ | 31 | A |
| | $T_C$=100°C | | 20 | A |
| Pulsed Drain Current [c] | | $I_{DM}$ | 89 | A |
| Continuous Drain Current [a] | $T_A$=25°C | $I_{DSM}$ | 11 | A |
| | $T_A$=70°C | | 9 | |
| Avalanche Energy L=0.3mH | | $E_{AS}$ | 44 | mJ |
| Power Dissipation [b] | $T_C$=25°C | $P_D$ | 41 | W |
| | $T_C$=100°C | | 16 | |
| Power Dissipation [a] | $T_A$=25°C | $P_{DSM}$ | 4.8 | W |
| | $T_A$=70°C | | 3.1 | |
| Operating Junction Temperature | | $T_J$ | -55 to 150 | °C |
| Storage Temperature Range | | $T_{STG}$ | -55 to 150 | °C |

## Thermal resistance ratings

| Single Operation | | | | | |
|---|---|---|---|---|---|
| Parameter | | Symbol | Typical | Maximum | Unit |
| Junction-to-Ambient Thermal Resistance [a] | t ≤ 10 s | $R_{\theta JA}$ | 20 | 26 | °C/W |
| | Steady State | | 45 | 56 | |
| Junction-to-Case Thermal Resistance | Steady State | $R_{\theta JC}$ | 2.2 | 3.1 | |

**Note:**

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm$^2$ area). The power dissipation $P_{DSM}$ is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C. The value is only for reference, any application depends on the user's specific board design.

b The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J$ =25°C, the maximum allowed junction temperature of 150°C.

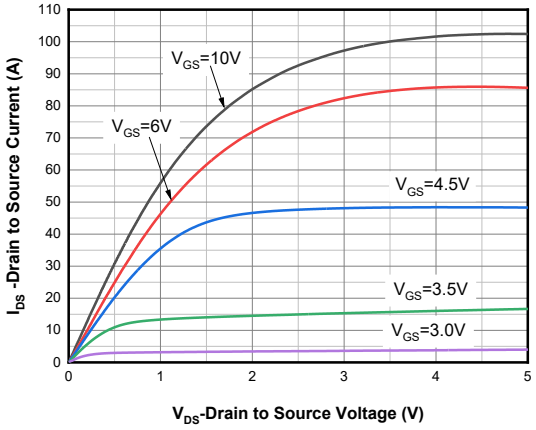
d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

e The parameter is not subject to production test – verified by design / characterization.

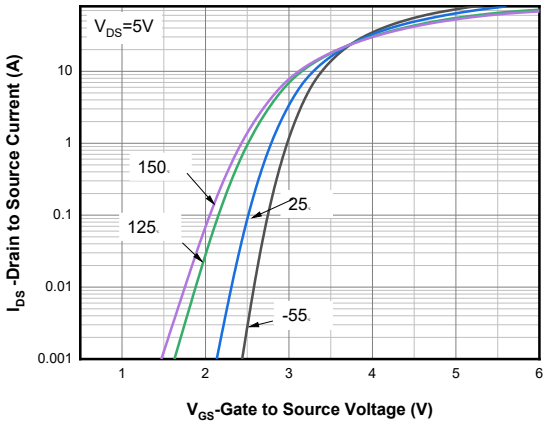
## Electronics Characteristics (Ta=25°C, unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250uA | 100 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 100V, $V_{GS}$ = 0V | | | 1 | μA |
| Gate-to-source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20V | | | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250uA | 1.5 | 2.0 | 2.5 | V |
| Drain-to-source On-resistance [d] | $R_{DS(on)}$ | $V_{GS}$ = 10V, $I_D$ = 15A | | 16 | 21 | mΩ |
| | $R_{DS(on)}$ | $V_{GS}$ = 4.5V, $I_D$ = 15A | | 23 | 34 | |
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | |
| Input Capacitance [e] | $C_{ISS}$ | $V_{GS}$ = 0V, f = 1.0MHz, $V_{DS}$ = 50 V | | 940 | | pF |
| Output Capacitance [e] | $C_{OSS}$ | | | 175 | | |
| Reverse Transfer Capacitance [e] | $C_{RSS}$ | | | 9.3 | | |
| Total Gate Charge [e] | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DD}$ = 50V, $I_D$ = 15A | | 17.6 | | nC |
| Total Gate Charge [e] | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DD}$ = 50V, $I_D$ = 15A | | 9.5 | | |
| Gate-to-Source Charge [e] | $Q_{GS}$ | | | 3.1 | | |
| Gate-to-Drain Charge [e] | $Q_{GD}$ | | | 4.8 | | |
| Gate Resistance | $R_g$ | f = 1MHz | | 0.7 | | Ω |
| **SWITCHING CHARACTERISTICS** [e] | | | | | | |
| Turn-On Delay Time | $td_{(ON)}$ | $V_{GS}$ = 10 V, $V_{DD}$ = 50 V, $I_D$=15A, $R_G$ = 1Ω | | 6 | | ns |
| Rise Time | tr | | | 12.6 | | |
| Turn-Off Delay Time | $td_{(OFF)}$ | | | 12.8 | | |
| Fall Time | tf | | | 3.0 | | |
| **BODY DIODE CHARACTERISTICS** | | | | | | |
| Forward Voltage [d] | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 15A | | 0.88 | 1.2 | V |
| Maximum Continuous Current [e] | $I_S$ | | | | 31 | A |
| Body Diode Reverse Recovery Time [e] | Trr | $I_F$=15A, dI/dt=100A/μs | | 30 | | ns |
| Body Diode Reverse Recovery Charge [e] | Qrr | | | 36 | | nC |

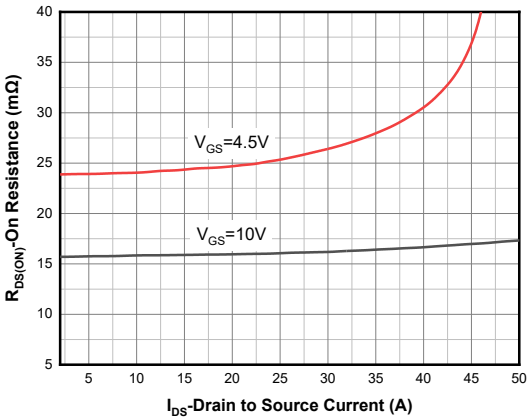
## Typical Characteristics (Ta=25°C, unless otherwise noted)



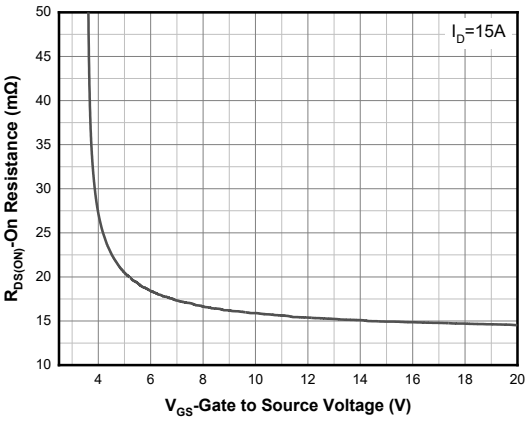

Output Characteristics [d]



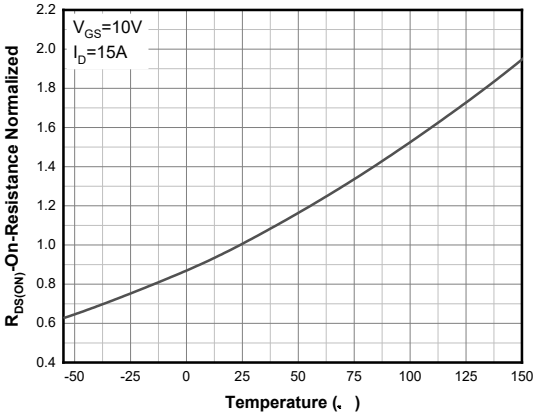

Transfer Characteristics [d]



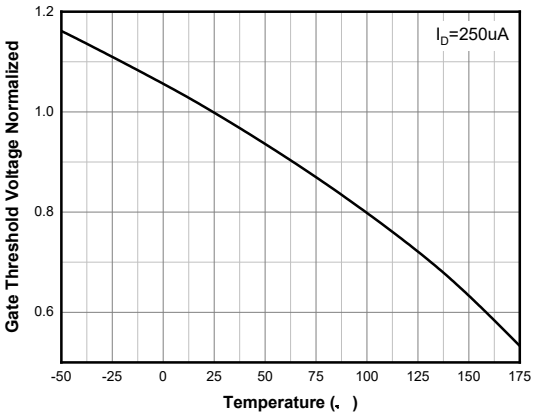

On-Resistance vs. Drain Current [d]



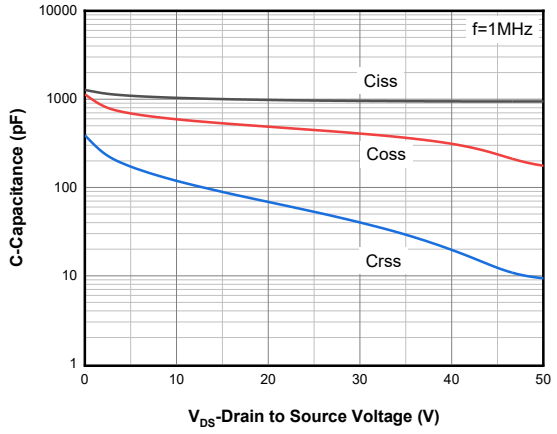

On-Resistance vs. Gate-to-Source Voltage [d]



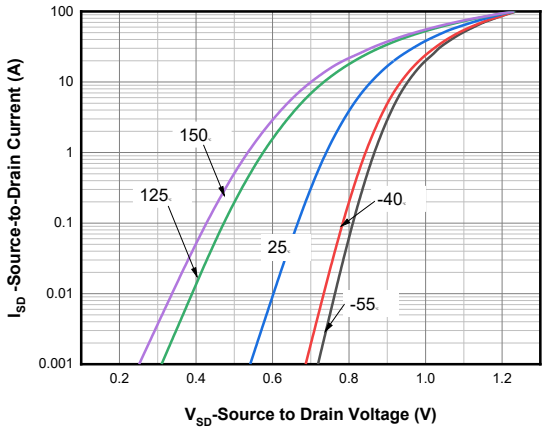

On-Resistance vs. Junction Temperature [d]



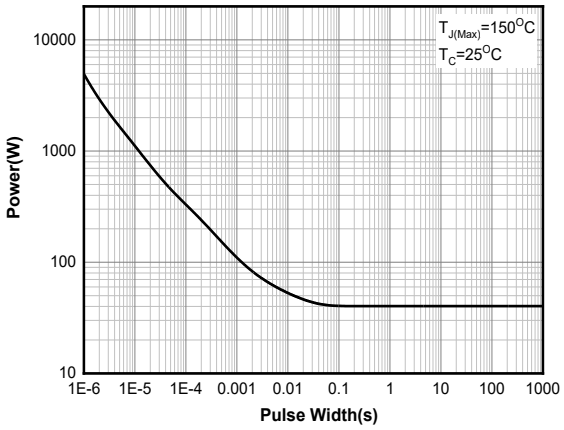

Threshold Voltage vs. Temperature



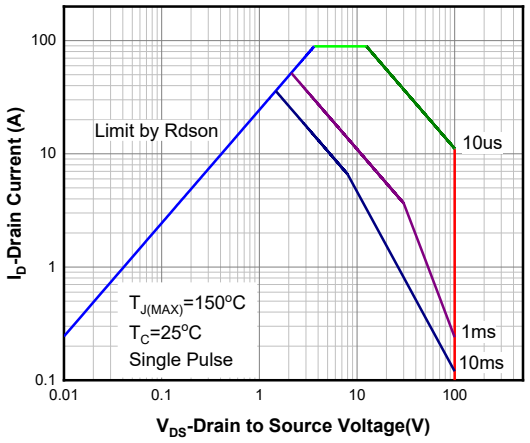

**Capacitance**



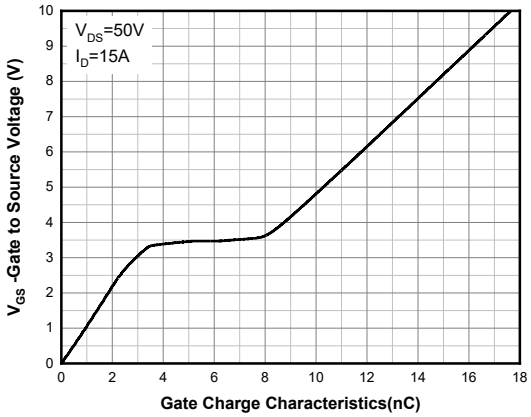

**Body Diode Forward Voltage [d]**



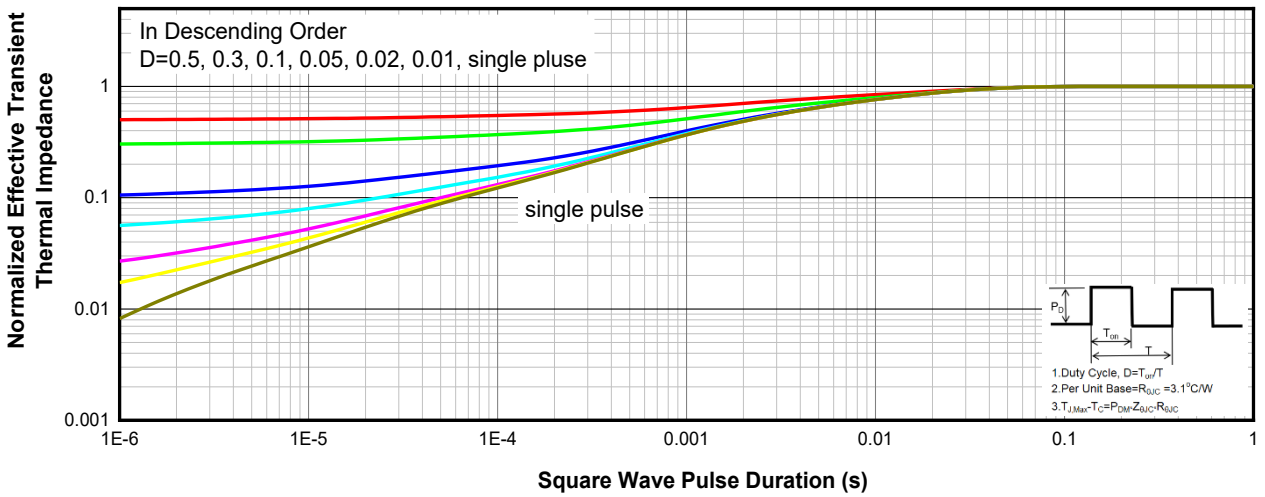

**Single Pulse power**



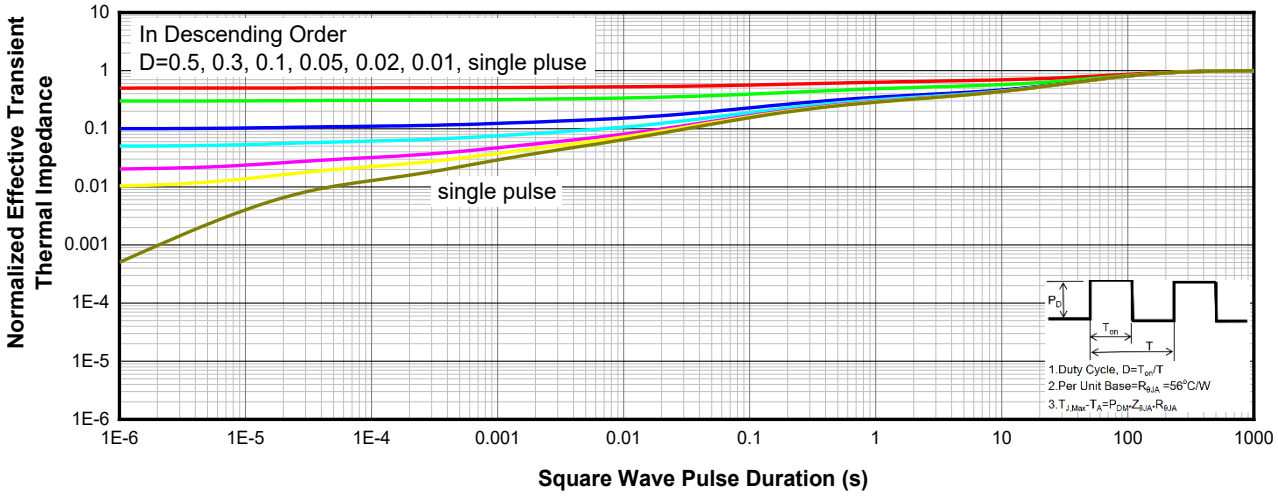

**Safe Operating Area**




**Gate Charge Characteristics**



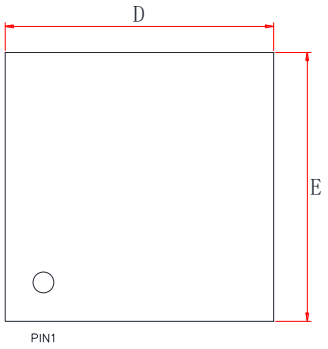

**Transient Thermal Response (Junction-to-Case)**



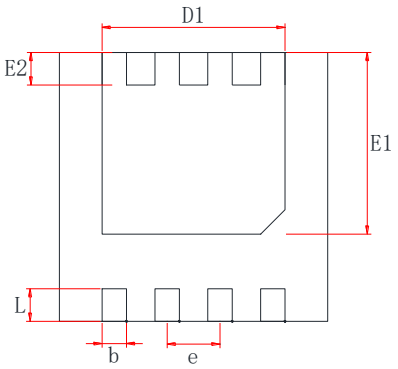

**Transient Thermal Response (Junction-to-Ambient)**

## PACKAGE OUTLINE DIMENSIONS

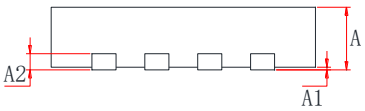
### DFN3333-8L



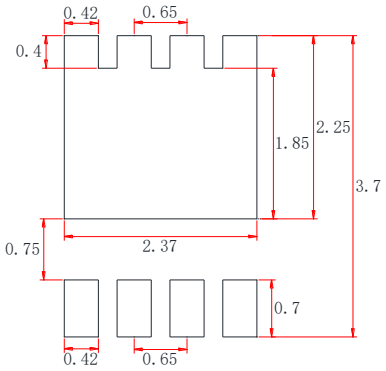

TOP VIEW




BOTTOM VIEW




SIDE VIEW

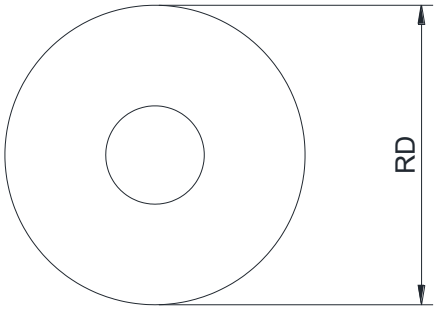



RECOMMENDED LAND PATTERN(unit:mm)

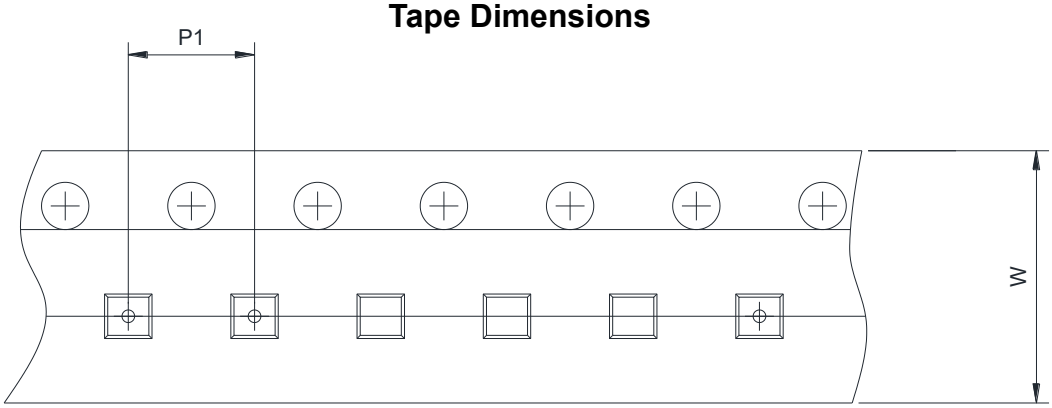
| Symbol | Dimensions in Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | - | - | 0.05 |
| A2 | 0.15 | 0.20 | 0.25 |
| b | 0.24 | 0.30 | 0.35 |
| D | 3.20 | 3.30 | 3.40 |
| D1 | 2.15 | 2.25 | 2.35 |
| E | 3.20 | 3.30 | 3.40 |
| E1 | 2.13 | 2.23 | 2.33 |
| E2 | 0.30 | 0.40 | 0.50 |
| e | 0.65 BSC | | |
| L | 0.30 | 0.40 | 0.50 |

## TAPE AND REEL INFORMATION

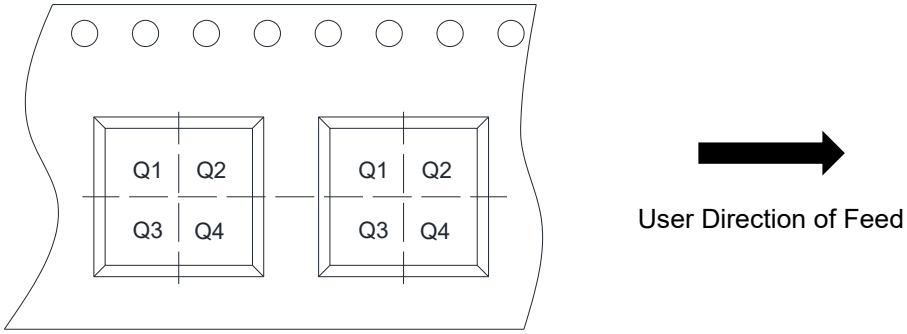
### Reel Dimensions




### Tape Dimensions




### Quadrant Assignments For PIN1 Orientation In Tape




| | | | | | |
|---|---|---|---|---|---|
| RD | Reel Dimension | ☐ 7inch | ☑ 13inch | | |
| W | Overall width of the carrier tape | ☐ 8mm | ☑ 12mm | ☐ 16mm | |
| P1 | Pitch between successive cavity centers | ☐ 2mm | ☐ 4mm | ☑ 8mm | |
| Pin1 | Pin1 Quadrant | ☑ Q1 | ☐ Q2 | ☐ Q3 | ☐ Q4 |